

### **ABSTRACT OF THE DISCLOSURE**

A semiconductor device having a memory array that includes a plurality of substantially parallel word lines, a plurality of substantially parallel bit lines, wherein each of the plurality of the word lines is substantially perpendicular to each of the plurality of the bit lines, a first dummy word line disposed at a periphery of the memory array, wherein the first dummy word line is substantially parallel to the plurality of word lines and overlaps at least two non-adjacent bit lines.

FINNEGAN  
HENDERSON  
FARABOW  
GARRETT &  
DUNNER LLP

1300 I Street, NW  
Washington, DC 20005  
202.408.4000  
Fax 202.408.4400  
[www.finnegan.com](http://www.finnegan.com)